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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/001,557	10/24/2001	Bohumil Lojek	ATM-204	6412

3897 7590 06/18/2003

SCHNECK & SCHNECK
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EXAMINER	
SOWARD, IDA M	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 06/18/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Offic Action Summary	Application No. 10/001,557	Applicant(s) LOJEK ET AL.	
	Examiner Ida M Soward	Art Unit 2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 August 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

This Office Action is in response to the Applicants' amendment filed August 9, 2002.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-8 rejected under 35 U.S.C. 103(a) as being unpatentable over Manley et al. (5,108,939) in view of Chang (6,160,287).

Regarding claims 1-8, Manley et al. disclose (Col. 6, lines 35-40) a semiconductor device with a layer of gate dielectric 503 formed in the substrate 501. (Col. 6, lines 40-45) A first layer 504 is then formed of a material suitable for use as a floating gate. (Col. 6, lines 60-65) An oxide 509 on the top and sidewall of floating gate 504. The exposed gate dielectric 503 is laid above drain 507. An oxide 509 on the top and sidewall of floating gate 504 slightly thickens the exposed gate oxide 503 above the source region 506. (Col. 5, lines 15-20) Openings 420, 421 are used to allow electrical contact between to-be-formed extensions 414, 415 and floating gate 408. (Col. 7, lines 20-25) An oxide layer 521 is formed on drain region 507. (Col. 7, lines 65-68) A second layer of dielectric 518 is then deposited on the structure of the floating gate. (Col. 7,

lines 55-60) An electrical connection is formed between floating gate 504 and floating gate extension spacer 515. (Col. 6, lines 15-30) The method for the formation of an EEPROM memory cell, and the resulting structure, provides for self-alignment of tunnel oxide region 411 to floating gate 408. (Col. 8, lines 10-20) A dielectric layer 518 is on the top of floating gate 504. (Abstract) A dielectric is then formed on the device in order to provide a dielectric over the drain region, which has a greater thickness than the tunnel dielectric underlying the floating gate extension, that is, the first insulating portion is thinner than the second insulating portion. However, Manley et al. fail to disclose a main gate region and a small sidewall spacer electrically coupled together by a connecting layer, wherein the connecting layer being formed over and in contact with both the small sidewall spacer and the main gate region. (Cols. 3-5, Figure 12, lines 44-67, 1-67 and 1-7, respectively) Chang discloses a main gate region of 60 and a small sidewall spacer 76 electrically coupled together by a connecting layer 80, wherein the connecting layer being formed over and in contact with both the small sidewall spacer and the main gate region. Since Manley et al. and Chang are from the same field of endeavor (flash memory structures), the purpose disclosed by Chang would have been recognized in the pertinent art of Manley et al. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the flash memory structure of Manley et al. by incorporating the connecting layer of Chang to reduce gate resistance (Col. 4, lines 4-7).

R spons to Arguments

Applicant's arguments with respect to claims 1-8 have been considered but are moot in view of the newly applied reference.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents are cited to further show the state of the art with respects to non-volatile memory devices:

Georgescu et al. (5,793,079)

Mehta et al. (6,060,766)

Roth et al. (5,616,941)

Wang et al. (5,703,388)

Wang (6,091,101).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ida M Soward whose telephone number is 703-305-3308. The examiner can normally be reached on Monday - Thursday, 6:30 am to 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 703-308-4905. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

ims
June 12, 2003

AMIR ZARABIAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800